Appl. No. 10/720,325
Examiner: Sarkar, Asok K, Art Unit 2891
In response to the Office Action dated May 10, 2005

Date: August 10, 2005
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AMENDMENTS TO THE SPECIFICATION

Please replace paragraph beginning on page 3, line 23, with the following amended paragraph:

To achieve these objects, a deep trench device structure and a method for making the same are provided. A deep trench is formed in a semiconductor substrate, and a buried trench capacitor is formed in the lower portion of the deep trench. A collar insulating layer is then formed lining the upper sidewall of the deep trench. A first conductive layer is deposited overlying the buried trench capacitor in the trench and surrounded by and lower than the collar insulating layer. A first portion of the collar insulating layer on the sidewall of the deep trench is then removed to expose a first portion of the semiconductor substrate while a second portion of the collar insulating layer remains to isolate a second portion of the semiconductor substrate. A second conductive layer is subsequently formed overlying the first conductive layer in the trench, wherein the second conductive layer is lower than the surface of the semiconductor substrate and a portion of the second conductive layer is isolated from the semiconductor substrate by the second portion of the collar insulating layer. Finally, a buried strap region is formed by thermal treatment in the semiconductor substrate directly in contact with the second conductive layer without isolation by the collar insulating layer.

Please replace paragraph beginning on page 8, line 29, with the following amended paragraph:

The exposed lining layer 53 is then etched with the remaining implanted undoped polysilicon or amorphous silicon layer 55 as a mask to expose collar insulating layers 50A and 50B on one sidewall of DT 41A and 41B. The exposed collar insulating layers 50A and 50B are subsequently removed with the remaining implanted undoped polysilicon or amorphous silicon layer 55 and the lining layer 53 as a mask to form lower collar insulating layers 50A' and 50B' on one sidewall of DT 41A and 41B respectively, as FIG. 7 shows. The remaining implanted undoped polysilicon or amorphous silicon layer 55 and the lining layer 53 are then removed, thereby forming DT 41A and 41B with high collar insulating layers 50A and 50B on one sidewall and lower collar insulating layers 50A' and 50B' of the opposite sidewall. As FIG.7 shows, a first portion of the collar insulating layers 50A and 50B are removed from the deep trench to form lower collar insulating layers 50A' and 50B' exposing a portion of the substrate 40. A second

portion of the collar insulating layers 50A and 50B remain to form high collar insulating layers and isolate the substrate 40.